CLAIMS

What is claimed is:

1. A system comprising a phased clock generator circuit, the phased clock generator circuit comprising:

an input clock terminal;

a plurality of output clock terminals;

a first counter circuit having a clock terminal coupled to the input clock terminal and further having N+1 output terminals, where N is an integer;

a divide-by-two register having a plurality of data input terminals coupled to N most significant output terminals of the first counter circuit, a clock terminal coupled to the input clock terminal, and a plurality of output terminals;

an adder circuit having a first plurality of data input terminals coupled to the N most significant output terminals of the first counter circuit, a second plurality of data input terminals coupled to N-1 most significant output terminals of the first counter circuit, and a plurality of output terminals;

a three-quarter register having a plurality of input terminals coupled to the output terminals of the adder circuit, and further having a plurality of output terminals;

a second counter circuit having a clock start terminal coupled to the input clock terminal, a plurality of clock stop terminals coupled to at least a subset of the output terminals of the divide-by-two register and the three-quarter register, and a plurality of output terminals; and

an output clock generator having a plurality of input terminals coupled to the output terminals of the second counter circuit, and further having a plurality of output terminals coupled to the output clock terminals.

2. The system of Claim 1, wherein the first counter circuit comprises:

a first oscillator circuit having an input terminal coupled to the clock input terminal and further having an output terminal; and

a first counter having an input terminal coupled to the output terminal of the first oscillator circuit and further having a plurality of output terminals coupled to the output terminals of the first counter circuit.

3. The system of Claim 2, wherein the second counter circuit comprises:

a second oscillator circuit having an input terminal coupled to the clock input terminal and further having an output terminal, the second oscillator circuit being implemented to oscillate with the same frequency as the first oscillator circuit;

a second counter having an input terminal coupled to the output terminal of the oscillator circuit and further having a plurality of output terminals;

a one-quarter comparator having a first set of input terminals coupled to a subset of the output terminals of the divide-by-two register, a second set of input terminals coupled to the output terminals of the second counter, and an output terminal coupled to a first one of the input terminals of the output clock generator;

a one-half comparator having a first set of input terminals coupled to the output terminals of the divide-by-two register, a second set of input terminals coupled to the output terminals of the second counter, and an output terminal coupled to a second one of the input terminals of the output clock generator; and

a three-quarter comparator having a first set of input terminals coupled to the output terminals of the three-quarter register, a second set of input terminals coupled to the output terminals of the second counter, and an output terminal coupled to a third one of the input terminals of the output clock generator.

4. The system of Claim 1, wherein the phased clock generator circuit further comprises a reset input terminal coupled to reset input terminals of the first counter circuit, the divide-by-two register, the three-quarter register, and the second counter circuit.

5. The system of Claim 1, wherein the phased clock generator circuit further comprises:

a reset input terminal; and

a flip-flop having a data input terminal coupled to the reset input terminal, a set terminal coupled to the data input terminal, a clock terminal coupled to the input clock terminal of the phased clock generator circuit, and an output terminal coupled to reset input terminals of the first counter circuit, the divide-by-two register, the three-quarter register, and the second counter circuit.

6. The system of Claim 1, wherein the first counter circuit comprises means for resetting itself after each M input clock periods, wherein M is an integer.

7. The system of Claim 6, wherein M is one of four and five.

8. The system of Claim 1, wherein the system comprises a programmable logic device (PLD), and the phased clock generator circuit is implemented using programmable logic of the PLD.

9. The system of Claim 8, wherein the PLD is a field programmable gate array (FPGA).

10. The system of Claim 8, wherein the PLD is a complex programmable logic device (CPLD).

11. The system of Claim 1, wherein the output clock generator comprises:

a first flip-flop having a data input terminal coupled to power high VDD, a clock terminal coupled to a first output terminal of the second counter circuit, a reset terminal coupled to a second output terminal of the second counter circuit, and an output terminal coupled to a first one of the output clock terminals; and

a second flip-flop having a data input terminal coupled to the power high VDD, a clock terminal coupled to a third output terminal of the second counter circuit, a reset terminal coupled to a fourth output terminal of the second counter circuit, and an output terminal coupled to a second one of the output clock terminals.

12. The system of Claim 11, wherein the output clock generator further comprises:

a third flip-flop having a data input terminal coupled to the power high VDD, a clock terminal coupled to a fifth output terminal of the second counter circuit, a reset terminal coupled to a sixth output terminal of the second counter circuit, and an output terminal coupled to a third one of the output clock terminals.

13. The system of Claim 1, wherein the output clock generator comprises:

a first flip-flop having a data input terminal coupled to power high VDD, a clock terminal coupled to a first output terminal of the second counter circuit, a reset terminal coupled to a second output terminal of the second counter circuit, and an output terminal coupled to a first one of the output clock terminals; and

a second flip-flop having a data input terminal coupled to the power high VDD, a clock terminal coupled to the input clock terminal, a reset terminal coupled to a third output terminal of the second counter circuit, and an output

terminal coupled to a second one of the output clock terminals.

14. A system providing from an input clock signal a plurality of phased output clock signals, the system comprising:

first counter means for counting a first number of counts between successive first edges of the input clock signal;

means for dividing the first number by four to provide a divided-by-four number;

means for dividing the first number by two to provide a divided-by-two number;

adder means for adding the divided-by-four number and the divided-by-two number to provide a three-quarter number;

second counter means for counting a second number of counts following each first edge of the input clock signal and comparing the second number with the divided-by-four number, the divided-by-two number, and the three-quarter number;

first pulse generator means for providing a first pulse on a first phased output clock signal in response to each first edge of the input clock signal;

second pulse generator means for providing a second pulse on a second phased output clock signal based on results of comparing the second number with the divided-by-four number;

third pulse generator means for providing a third pulse on a third phased output clock signal based on results of comparing the second number with the divided-by-two number; and

fourth pulse generator means for providing a fourth pulse on a fourth phased output clock signal based on results of comparing the second number with the three-quarter number.

15. The system of Claim 14, further comprising reset means for resetting the first counter means, the second counter means, the first pulse generator means, the second pulse generator means, the third pulse generator means, and the fourth pulse generator means.

16. The system of Claim 14, wherein the first counter means comprises means for resetting itself after each M input clock periods, wherein M is an integer.

17. The system of Claim 16, wherein M is one of four and five.

18. The system of Claim 14, wherein each of the first, second, third, and fourth phased output clock signals has a pulse width the same as a pulse width of the input clock signal.

19. The system of Claim 14, wherein each of the first, second, third, and fourth phased output clock signals has a 50 percent duty cycle.

20. The system of Claim 14, further comprising means for enabling duty cycle correction for the first, second, third, and fourth phased output clock signals.

21. A method of providing from an input clock signal a plurality of phased output clock signals, the method comprising:

counting a first number of counts between successive first edges of the input clock signal;

dividing the first number by four to provide a divided-by-four number;

dividing the first number by two to provide a divided-by-two number;

adding the divided-by-four number and the divided-by-two number to provide a three-quarter number;

counting a second number of counts following each first edge of the input clock signal and comparing the second number with the divided-by-four number, the divided-by-two number, and the three-quarter number;

providing a first pulse on a first phased output clock signal in response to each first edge of the input clock signal;

providing a second pulse on a second phased output clock signal based on results of comparing the second number with the divided-by-four number;

providing a third pulse on a third phased output clock signal based on results of comparing the second number with the divided-by-two number; and

providing a fourth pulse on a fourth phased output clock signal based on results of comparing the second number with the three-quarter number.

22. The method of Claim 21, wherein the counting the first number of counts is repeated every M periods of the input clock signal, wherein M is an integer.

23. The method of Claim 22, wherein M is one of four and five.

24. The method of Claim 21, wherein the steps of the method are performed by a circuit implemented in a programmable logic device (PLD).

25. The method of Claim 24, wherein the PLD is a field programmable gate array (FPGA).

26. The method of Claim 24, wherein the PLD is a complex programmable logic device (CPLD).

27. The method of Claim 21, wherein the first number has 2 to the power of 8 possible values.

28. The method of Claim 21, wherein the first edges are rising edges.

29. The method of Claim 21, wherein each of the first, second, third, and fourth phased output clock signals has a pulse width the same as a pulse width of the input clock signal.

30. The method of Claim 21, wherein each of the first, second, third, and fourth phased output clock signals has a 50 percent duty cycle.

31. The method of Claim 21, further comprising enabling duty cycle correction for the first, second, third, and fourth phased output clock signals.